Computer Architecture - Exam 1  
Originally done by Liz Shackleford

Chapter 1

* What is Micro Programming?
* What is the function of the control unit?
* Basic IAS Structure
* MAR/MBR
* Wafers/Chips
* Moore's Law
* What is an embedded system?
* What is cloud computing?
* What is the Internet of Things?

Chapter 2 - Performance Issues

* Performance Balance
  + Wider vs Deeper memories
* IO Data Rates
* Power
* RC Delays
* Amdahl's Law
* GPU
* (Ignore Little's Law)
* AM, GM, HM
  + Impact of performance evaluation
* Benchmarks and their role

Chapter 3 - Buses

* Memory Read/Write cycles
* Figure 3.5 - be familiar with that
* Classes of Interrupts
  + Soft, hard, timer, IO
* When is an interrupt checked? Or detected?
  + Figure 3.9
* Handling of multiple Interrupts
* Data Bus, Address Bus, Control Bus
* Hierarchical Bus Configuration and elements of bus design
* Arbitration - centralized and distributed
* Synchronous and Asynchronous Buses
* Multi core QPI configuration (concepts here, not details)
* PCI and PCI Express (concepts only, not details)

Chapter 4 - Cache - lots of attention on

* Access/Cycle/Transfer time
* Sequential/Direct/Random Access
* Direct Mapping, Associative Mapping, Set Mapping
  + Be able to do problems about these
* Set-Associative
* Write Thru/Back
* Unified and Split Cache Decision
* Replacement Algorithms
  + LRU
  + FIFO
  + LFU
  + Random
* Victim Cache
* Write Back Buffer
* Hit Ratios
* Cost Analysis
  + Cache
  + Memory

Chapter 5 -  Internal Memory

* DRAM, EEPROM, PROM, Flash
  + How these function
* 1-Tcell/6-Tcell (SRAM)
* Charging, refresh cycle
* Figure 5.3 DRAM org
* Error correction codes
  + Hard, soft failures
  + Parity
  + Hamming codes
* SDDRam, DDR SDRAM (mainly concepts, not details)